

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A compressor of a multiplier comprising:  
2 a first compressor, wherein said first compressor comprises:  
3 a first plurality of inputs;  
4 a first summation output;  
5 a first carry bit output; ~~and~~  
6 a first plurality of transistor paths connecting each of  
7 said first plurality of inputs to said summation output, wherein a  
8 first compressor critical transistor stage path level within said  
9 first compressor is less than seven;  
10 a second carry bit output;  
11 a second plurality of transistor paths connecting each of  
12 said first plurality of inputs to said second carry bit  
13 output; and  
14 a successive compressor, wherein said successive compressor  
15 comprises:  
16 a second plurality of inputs;  
17 a second summation output; and  
18 said compressor of a multiplier further comprising:  
19 a plurality of successive transistor paths connecting at  
20 least one of said first plurality of inputs to said first carry bit  
21 output of said first compressor, connecting said first carry bit  
22 output to at least one of said second plurality of inputs between  
23 said first compressor and said second compressor and connecting at  
24 least one of the second plurality of inputs to said second  
25 summation output of said successive compressor, wherein a  
26 successive compressor critical transistor stage path level within  
27 said successive compressor is less than eight;

28       wherein each of said first plurality of transistor paths, each  
29 of said second plurality of transistor paths, and each of said  
30 plurality of successive transistor paths comprises a plurality of  
31 switches and a plurality of inverters;  
32       wherein said switches and said inverters form a plurality of  
33 logic stages for each of said first plurality of inputs; and  
34       wherein a first compressor critical logic stage path level is  
35 three within said first compressor and a successive compressor  
36 critical logic stage path level is three within said successive  
37 compressor.

2 to 4.     (Canceled)

1     5.     (Currently Amended) The compressor of claim 4 1, wherein at  
2     least one of said logic stages for at least one of said first  
3     plurality of inputs is a transfer gate XOR stage and at least one  
4     of said logic stages for at least one of said first plurality of  
5     inputs is a transfer gate XNOR stage.

1     6.     (Currently Amended) The compressor of claim 3 1, wherein when  
2     one of said first plurality of inputs is connected to a source of  
3     one said switches, said input is not connected to a gate of another  
4     of said switches, and when one of said first plurality of inputs is  
5     connected to a gate of one said switches, said input is not  
6     connected to a source of another of said switches.

1     7.     (Currently Amended) The compressor of claim 3 1, wherein a  
2     drain of each of said switches is not connected to a source of  
3     another of said switches.

1     8.     (Currently Amended) The compressor of claim 4 1, wherein when  
2     one of said inverters within one of said logic stages is connected

3 to a source of one of said switches within the same logic stage as  
4 said inverter, said inverter is not connected to a gate of another  
5 of said switches within the same logic stage as said inverter, and  
6 when one of said inverters within one of said logic stages is  
7 connected to a gate of one of said switches within the same logic  
8 stage as said inverter, said inverter is not connected to a source  
9 of another of said switches within the same logic stage as said  
10 inverter.

9. (Canceled)

1 10. (Currently Amended) ~~The A compressor of claim 2,~~ a multiplier  
2 comprising:  
3 a first compressor, wherein said first compressor comprises:  
4 a first plurality of inputs;  
5 a first summation output;  
6 a first carry bit output;  
7 a first plurality of transistor paths connecting each of  
8 said first plurality of inputs to said summation output, wherein a  
9 first compressor critical transistor stage path level within said  
10 first compressor is less than seven;  
11 a second carry bit output;  
12 a second plurality of transistor paths connecting each of  
13 said first plurality of inputs to said second carry bit  
14 output; and  
15 a successive compressor, wherein said successive compressor  
16 comprises:  
17 a second plurality of inputs;  
18 a second summation output; and  
19 said compressor of a multiplier further comprising:  
20 a plurality of successive transistor paths connecting at  
21 least one of said first plurality of inputs to said first carry bit

22 output of said first compressor, connecting said first carry bit  
23 output to at least one of said second plurality of inputs between  
24 said first compressor and said second compressor and connecting at  
25 least one of the second plurality of inputs to said second  
26 summation output of said successive compressor, wherein said first  
27 compressor critical transistor stage path level within said first  
28 compressor is six and said successive compressor critical  
29 transistor stage path level within said successive compressor is  
30 seven.

1 11. (Original) The compressor of claim 10, wherein a number of  
2 said first plurality of inputs is five.

1 12. (Currently Amended) The compressor of claim 4 1, wherein a  
2 first compressor critical logic stage path level is less than four  
3 and a successive compressor critical logic stage path level is less  
4 than four.

1 13. (Currently Amended) The compressor of claim 2 1, wherein a  
2 number of binary ones in the first plurality of inputs is the sum  
3 of two times the first carry bit output, two times the second carry  
4 bit output, and the summation output.

1 14. (Original) The compressor of claim 13, wherein the summation  
2 output, the second carry bit output, and the first carry bit  
3 output, are logically expressed as

4 
$$So = ((Bi \oplus Ci) \oplus (Di \oplus Ai)) \oplus Xi;$$

5 
$$Co = ((Bi \oplus Ci) \oplus (Di \oplus Ai)) \cdot Xi + ((Bi \oplus Ci) \oplus (Di \oplus Ai))$$
  
6 
$$\cdot Ai; \text{ and}$$

7 
$$Xo = (Bi \oplus Ci) \cdot Di + (Bi \oplus Ci) \cdot Bi.$$

Claims 15 to 36. (Canceled)